**Stu.ID: Name:**

**Answers Sheet of Lab 2: Logic Gates**

**Task 2 – Construct and verify the NAND Gate**

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

**Task 3 – Construct and verify the NOR Gate**

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

**Task 4 – Construct and verify the XOR Gate (Mandatory for Lab 2B):**

|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 0 |

**[Bonus] Task 5 – Construct and verify the Half Adder (Mandatory for Lab 2B):**

**Half Adder Circuit:**

**Case 1:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A = 0** | **B = 0** | **Carry = 0** | **Sum = 0** | **Decimal = 0** |

**serial monitor:**

**LEDs status:**

**Case 2:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A = 0** | **B = 1** | **Carry = 0** | **Sum = 1** | **Decimal = 1** |

**serial monitor:**

**LEDs status:**

**Case 3：**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A = 1** | **B = 0** | **Carry = 0** | **Sum = 1** | **Decimal = 1** |

**serial monitor:**

**LEDs status:**

**Case4：**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A = 1** | **B = 1** | **Carry = 1** | **Sum = 0** | **Decimal = 2** |

**serial monitor:**

**LEDs status:**

**Please Submit your Answer Sheet on Canvas/Assignments/Lab 2**